Svvptc ratification plan

- Svvptc extension enables OS to elide memory-management fences when making PTEs valid
  - Motivated by performance gains by eliding the memory management fences
  - Extension does not introduce new CSRs/CSR-fields or new instructions
- POC Goals
  - Provide a simulator for software development
  - Updated Linux memory management
  - Lmbench and LTP tests to demo benefits
- POC
  - Simulator: QEMU
  - OS: Linux
  - Tests: Lmbench, LTP
- No updates needed to sail, qemu, or riscv-arch-tests
- Draft specification: [https://github.com/riscv/riscv-svvptc](https://github.com/riscv/riscv-svvptc)
- Jira: [https://jira.riscv.org/browse/RVS-1984](https://jira.riscv.org/browse/RVS-1984)
- Requesting Tech chairs approval for the Svvptc extension ratification plan

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**Timeline**

- Fast Track Approved & AR started: 12/12/2023
- Members review started: 12/12/2024
- Expected AR Complete: 2/15/2024
- Freeze: 4/30/2024
- Public Review Complete: 6/1/2024
- Ready for Ratification Ready Vote: 6/5/2025
- PoC: Ready Vote

**Dates**

- Q4-2023
- Q2-2024
| Test                     | Gain | # of SFENCE.VMA |
|--------------------------+------|-----------------|
| Kernel boot              | 6%   | 50535 -> 8768   |
| ltp - mmapstress01       | 8%   | 44978 -> 6300   |
| lmbench - lat_pagefault  | 20%  | 665254 -> 832   |
| lmbench - lat_mmap       | 5%   | 546401 -> 718   |