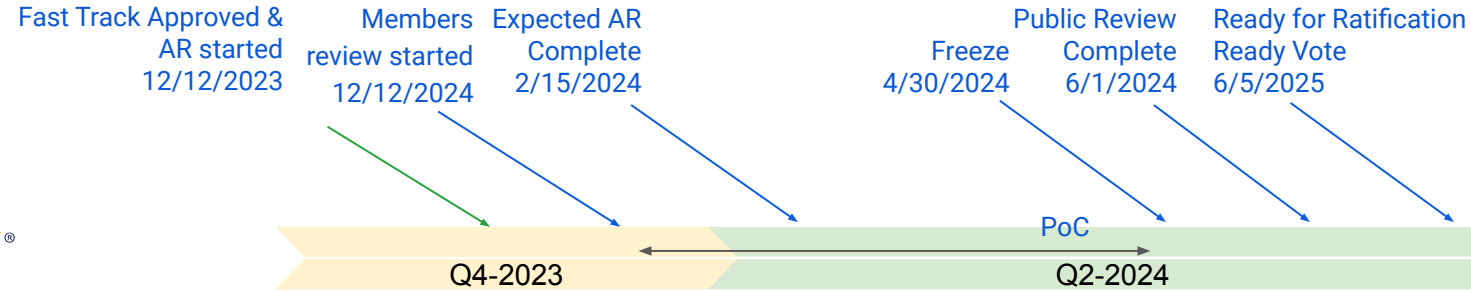
Svvptc Fast-track extension

Presented by: Ved Shanbhogue

Tech Chairs Review

Svvptc ratification plan

- Svvptc extension enables OS to elide memory-management fences when making PTEs valid
  - Motivated by performance gains by eliding the memory management fences
  - Extension does not introduce new CSRs/CSR-fields or new instructions
- POC Goals
  - Provide a simulator for software development
  - Updated LInux memory management
  - Lmbench and LTP tests to demo benefits
- POC
  - Simulator: QEMU
  - OS: Linux
  - Tests: lmbench, LTP
- No updates needed to sail, qemu, or riscv-arch-tests
- Draft specification : https://github.com/riscv/riscv-svvptc
- Jira :https://jira.riscv.org/browse/RVS-1984
- Requesting Tech chairs approval for the Svvptc extension ratification plan



Test	Gain	# of SFENCE.VMA
Kernel boot	6%	50535 -> 8768
ltp - mmapstress01	8%	44978 -> 6300
lmbench - lat pagefault	20%	665254 -> 832
lmbench - lat_mmap	5%	546401 -> 718