SIG-HPC Charter

This charter describes operations as a RISC-V SIG. The Focus section below describes what is in and out of scope, and Governance section describes how our operations are consistent with RISC-V foundation policies with links to more detailed documents.

Mission: Provide a global forum for technical and strategic high performance computing, systems and components (processors, accelerators, etc.) targeting large scale performance (tera-, peta-, exascale, and beyond) and power targets (any data and compute intensive domains), imperatives to leverage and enable RISC-V.

Motivation

The demand for computing continues to grow with the explosive growth in data. This demand spans everything from traditional large-scale HPC, as well as emerging domains like High Performance Data Analytics (HPDA). These systems are high performance, but also power constrained. Regardless of the deployment, supercomputer center, public cloud or even the edge, we must charter a path for hardware and software to extend RISC-V into this broad and growing domain. Starting from the top of the domain, there are traditional HPC workloads that are expanding into AI/ML/DL and beyond. Supporting this ecosystem will enable a trickle down of technology to other domains. From the bottom, enabling embedded HPC domains to flourish is also critical and providing a common ecosystem for data and compute to transit from the bottom to the top may provide additional system co-design opportunities.

HPC has flourished in the open source software community and has the appropriate technologies, adding RISC-V enables true software/hardware co-design capabilities for future systems. Given the genesis of RISC-V, this area has received less attention than others in the RISC-V ecosystem. There are two main thrusts to enable a vibrant HPC RISC-V ecosystem: Technical and Business imperatives. Instead of relying on organic growth driven by current needs, this SIG provides a structured and planned approach that enables many different domains with different requirements.

The SIG-HPC will provide a broader view of the RISC-V ecosystem and support several technical and non-technical working groups that support this vision of RISC-V solutions deploying in all levels of the hardware stack, in HPC and supercomputers, all with compute (and data) intensive requirements.

Focus

In addition to the RISC-V HPC related projects, there are key focus areas on the technical and business side that will facilitate the growth of the RISC-V ecosystem.

From a technology perspective, there are many imperatives to align and enable across the software and hardware stack:

· Compute intensive applications and application domains HPC, including HPDA (AI/ML/DL).

· System software stack from applications, middleware and frameworks, to toolchains (compilers, debuggers, etc.), and board support packages (BSPs).

· Software ecosystem alignment and roadmap (e.g., for RISC-V FORTRAN, Vector pragmas, autovectorizers, OpenMP, MPI, BLAS, TensorFlow, etc.)

· Communicating ISA standards alignment for HPC (e.g., Vector and other ISA extensions for Supercomputers, 57b, 64b, 128b addressing, reproducible floating-point and/or other floating point standards (RISC-V bfloat16, POSITS) , etc.)

· Enabling current and future applications with simulation, emulation, verification and compliance testing capabilities.

· Enabling accelerators for a variety of domains (software and hardware) with well thought out interfaces, ISA extensions and other infrastructure and specifications.

· Engaging with physical design and foundries to facilitate implementation with new and existing technologies and IP.

From a business, there are many opportunities to develop awareness and collaboration, such as:

· Engage and represent RISC-V in compute intensive industry and academic events, including HPC, AI/ML/DL, and embedded domains.

· Identify key industrial and academic partners with aligned interest around a common set of features for high performance, low power systems. This would enable repurposing of the hardware across many application/software domains.

· Navigating international political and legal requirements and restrictions

· Support global technology independence with a RISC-V ecosystem roadmap and partners.

In scope

Terminology note: SIG-HPC uses the term "end user" to describe the humans who use high performance computing applications. This definition can be extended to companies or industries that rely on HPC.

When we use the word "HPC" within this group, it is defined to be inclusive of concerns that affect the entire ecosystem (software and hardware). Furthermore, we include all applications and use cases that require high performance and can be deployed as a single small system, all the way up to a massive supercomputer. The common elements are the algorithms and system requirements for the applications are shared, while the size, weight and performance (SWaP) may impact the deployment. Different deployments may require different solutions, which must be considered for the RISC-V specifications.

SIG-HPC will consider proposals from its members or delegated tasks from the RISC-V TOC that are consistent with the mission, including the following activities:

- Publish educational resources on RISC-V HPC
    - Videos and/or slides from invited presentations by HPC providers and use cases
    - Answer the following questions (referring to already existing resources where possible):
        - What RISC-V HPC ecosystem components exist and possible academic and industrial partners?
        - What existing and emerging applications and domains are covered in HPC?
        - What additional measures are needed, specific to HPC, in highly regulated environments?
    - Personas and use cases
    - Common vocabulary to talk about and understand HPC
    - RISC-V project ecosystem & landscape
    - Define HPC scenarios (e.g. cores, peripherals, accelerators, system software, applications, etc.)
    - Block architecture(s) for HPC
    - Highlight trade-offs
    - Best practices and anti-patterns (potentially highlighting where there is disagreement on these)

- HPC assessments of specific proposals or projects
- HPC software and hardware ecosystem and roadmaps
- Identify projects for consideration for RISC-V
- Cross-pollinate knowledge by participating and inviting people from other projects and SIGs to share HPC practices
- Integrate relevant external standards, such as from Vector extensions or processor and accelerator interfaces, and others, as part of educational resources and/or SIG processes

Given that the group is composed of volunteers, specific requests from the TSC may be queued according to the bandwidth of the group. The co-chairs will facilitate prioritization under the guidance of the SIG-HPC TSC liaison.

Out of scope

- Not a standards body: We won't be creating standards. We do create technical workgroups that will create standards and suggestions to current workgroups
- Not an umbrella organization: We interact with other groups for knowledge sharing, not decision-making.
- Not a compliance body
- Not a certification board for HPC of individual projects
- We will not
    - answer any specific questions regarding the state of HPC of any project or product

Governance

HPC must be addressed at all levels of the stack and across the whole ecosystem, so the group seeks to encourage participation and membership across a wide range of roles, from diverse companies and organizations.

Cross-group relationships

To focus our efforts, we avoid duplication by developing relationships with other groups that focus on a particular technology (such as other software HPC SIGs) or have a broader mandate (such as government organizations). Group relationships may be within the RISC-V International organization or external to RISC-V.

As a guide to visitors, we maintain the list of groups in the SIG README.

Co-chairs are responsible to ensure periodic cross-group knowledge sharing, which is accomplished by cross-group membership, invitation to present at a SIG meeting and/or offering to present to the related group.

Operations

SIG-HPC operations are consistent with standard SIG operating guidelines provided by the RISC-V Technical Steering Committee TSC .

Full details of process and roles are linked from governance README.