RISC-V Trace & Diagnostic Data
Transport Encapsulation
Ratification Plan

Presented by: Iain Robertson, E-Trace-Encap TG

Tech Chairs Review
Background

The Efficient Trace for RISC-V (E-trace) standard defines packet payloads for instruction and data trace but does not fully define:

- How this should be encapsulated for transport, nor
- How instruction and data trace should be differentiated

(deliberate scoping choice to focus on packet payloads only)

Although primary motivation was encapsulation for E-Trace, it is

- Payload agnostic so can be used for any kind of data
- Suitable for various transport mechanisms, including AMBA ATB and Siemens messaging infrastructure
Overview

● A simple packet encapsulation in two forms:
  ○ Normal packets for trace and other data payloads
    ■ 1 byte header defines packet length (max 31B), some routing options, presence of timestamp
    ■ SrcID (0-16 bits, fixed per system, discoverable)
    ■ Optional timestamp (N bytes, fixed per system, discoverable)
    ■ type (default 2 bits, may be more per source if discoverable)
    ■ Payload
  ○ Null packets for idles and synchronization
    ■ Single byte header with length = 0 only

● Synchronization sequence for framed or unframed data
Design Considerations

- Simple
- Directly support existing E-Trace packet formats
- Not limited to E-Trace
- Compatible with existing commonly used transport infrastructure
  - AMBA ATB
  - Siemens messaging infrastructure
- Leverage proven solutions
  - Siemens solution (in use for > 10 years) is fully compliant
# Key Milestones

Jira Spec [https://jira.riscv.org/browse/RVS-1933](https://jira.riscv.org/browse/RVS-1933)

<table>
<thead>
<tr>
<th>Key Milestones</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plan Approval</td>
<td>20-Dec-2023</td>
</tr>
<tr>
<td>Internal Review Start</td>
<td>20-Dec-2023</td>
</tr>
<tr>
<td>Architecture Review Request</td>
<td>20-Dec-2023</td>
</tr>
<tr>
<td>Freeze Milestone</td>
<td>20-Mar-2024</td>
</tr>
<tr>
<td>Public Review Start</td>
<td>20-Mar-2024</td>
</tr>
<tr>
<td>Ratification-Ready Milestone</td>
<td>03-May-2024</td>
</tr>
<tr>
<td>TSC Approval</td>
<td>17-May-2024</td>
</tr>
<tr>
<td>Board Ratification</td>
<td>23-May-2024</td>
</tr>
</tbody>
</table>
Proof-of-concept

SystemVerilog model showing

- Encapsulation, transport and de-encapsulation of payload
- Correct synchronization to stream of packets transmitted as bytes or bits

Can be easily constructed reusing much existing testbench code with minimal required changes, as differs from existing Siemens messaging infrastructure in only a few small ways

- SrcID can be omitted (Siemens always present)
- Timestamp length N bytes (Siemens always 2 bytes)
- type can be > 2 bits (Siemens always 2 bits)
- Unframed synchronization (new)
Non-ISACE Freeze Checklist

<table>
<thead>
<tr>
<th>Non-ISA Item</th>
<th>Task Description</th>
<th>Plan</th>
<th>Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Construct SystemVerilog SVUnit TB using existing VIP with a few enhancements</td>
<td>Planned</td>
<td>Iain Robertson / Siemens</td>
</tr>
</tbody>
</table>
| Tests        | • Encapsulate random payload, transport with sync and decode, across range of allowed encapsulation parameters (field lengths, etc)  
• Test synchronization boundary cases with pathological payloads | Planned | Iain Robertson / Siemens |
Summary

- Draft specificion: https://github.com/riscv-non-isa/e-trace-encap/tree/main
- Ratification Plan: https://docs.google.com/document/d/1RCOl4qtIhPY7jlmPqP5ylQq0juIF9tPLVCPVp74BEEg/edit
- Status checklist: https://docs.google.com/spreadsheets/d/1thQxKPo18UR9xNRh96e5xEA4GPWxabeSCvquS2wkB0/edit#gid=257164574

Spec is ready for review
Proof of Concept needs to be developed, but is very close to Siemens messaging scheme which has been in use for over 10 years

Goal is to freeze the extension by 20-Mar-2024 and ratify by 23-May-2024.